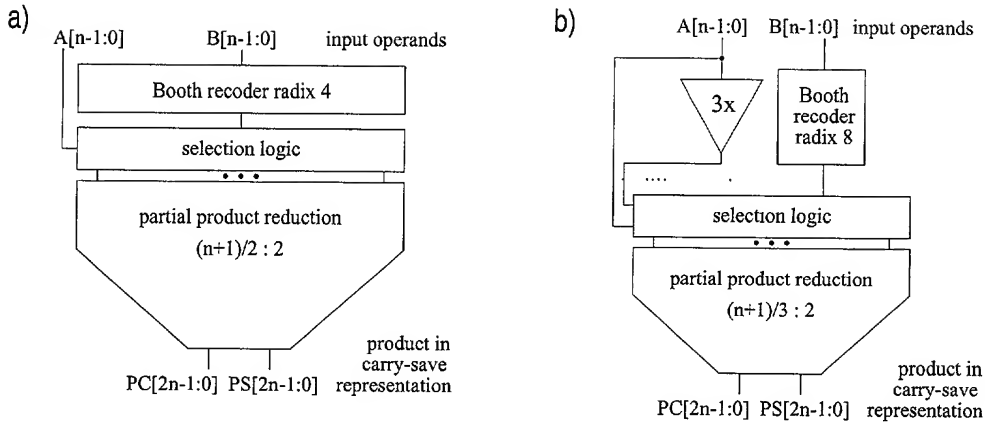

Figure 1: Block digrams of partial product generation for prior art a) Booth radix-4 and b) Booth radix-8 multipliers.

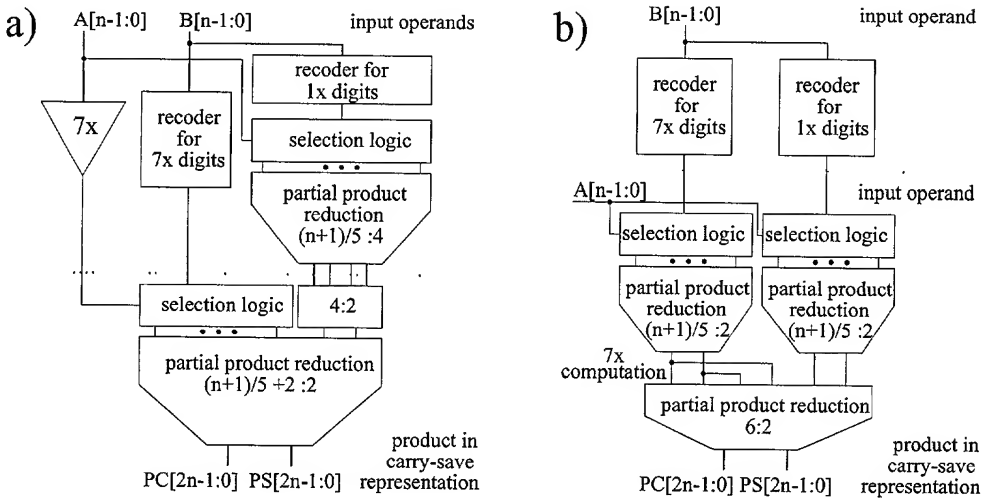

Figure 2: Simplified block digrams of partial product generation for a) radix-32 recoding with precomputation of $7x$ and b) preferred embodiment radix-32 encoding with postcomputation of $7x$ multipliers.

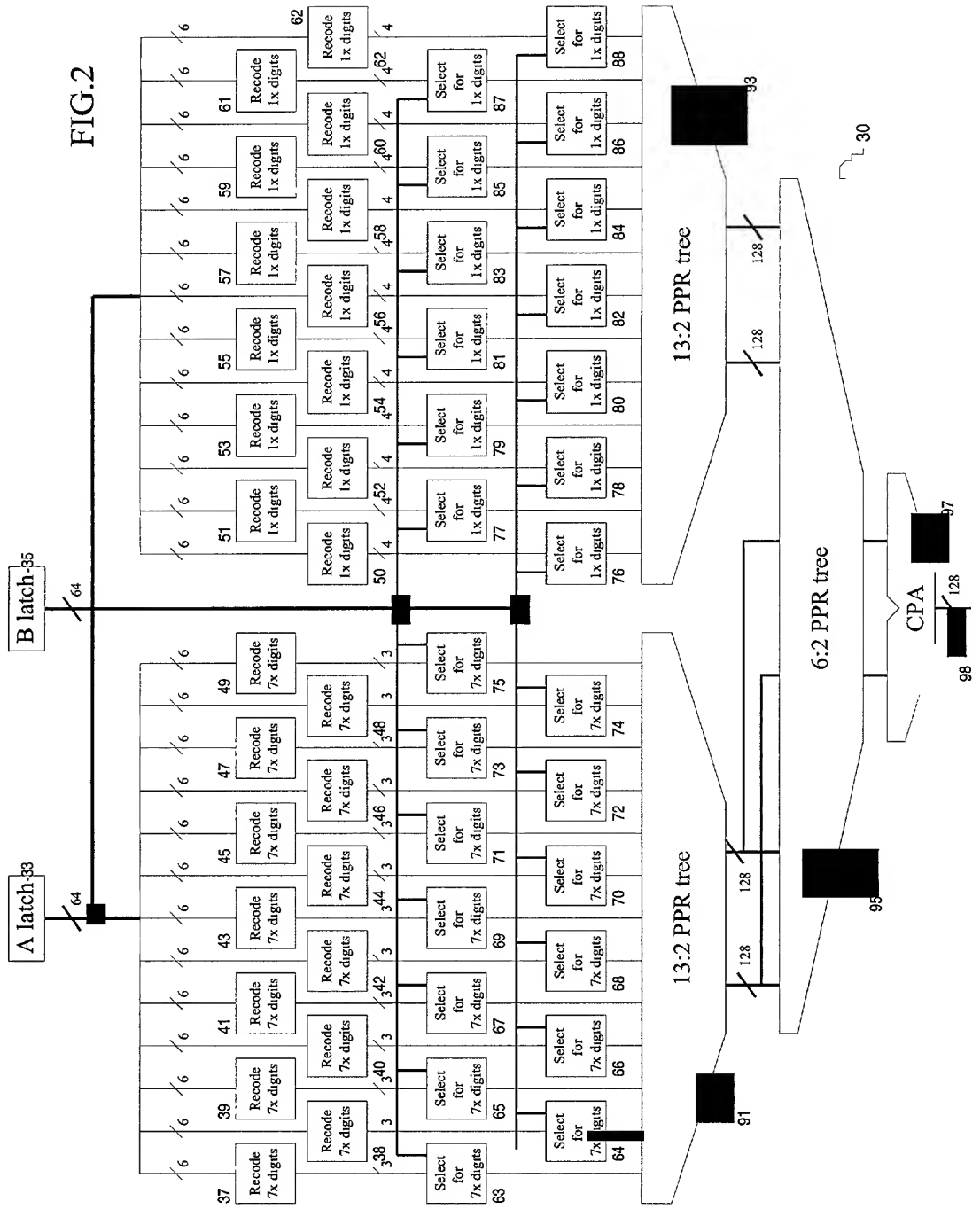

Figure 3: Block diagram of the preferred embodiment of the invention for a multiplier bit width of $p = 64$.

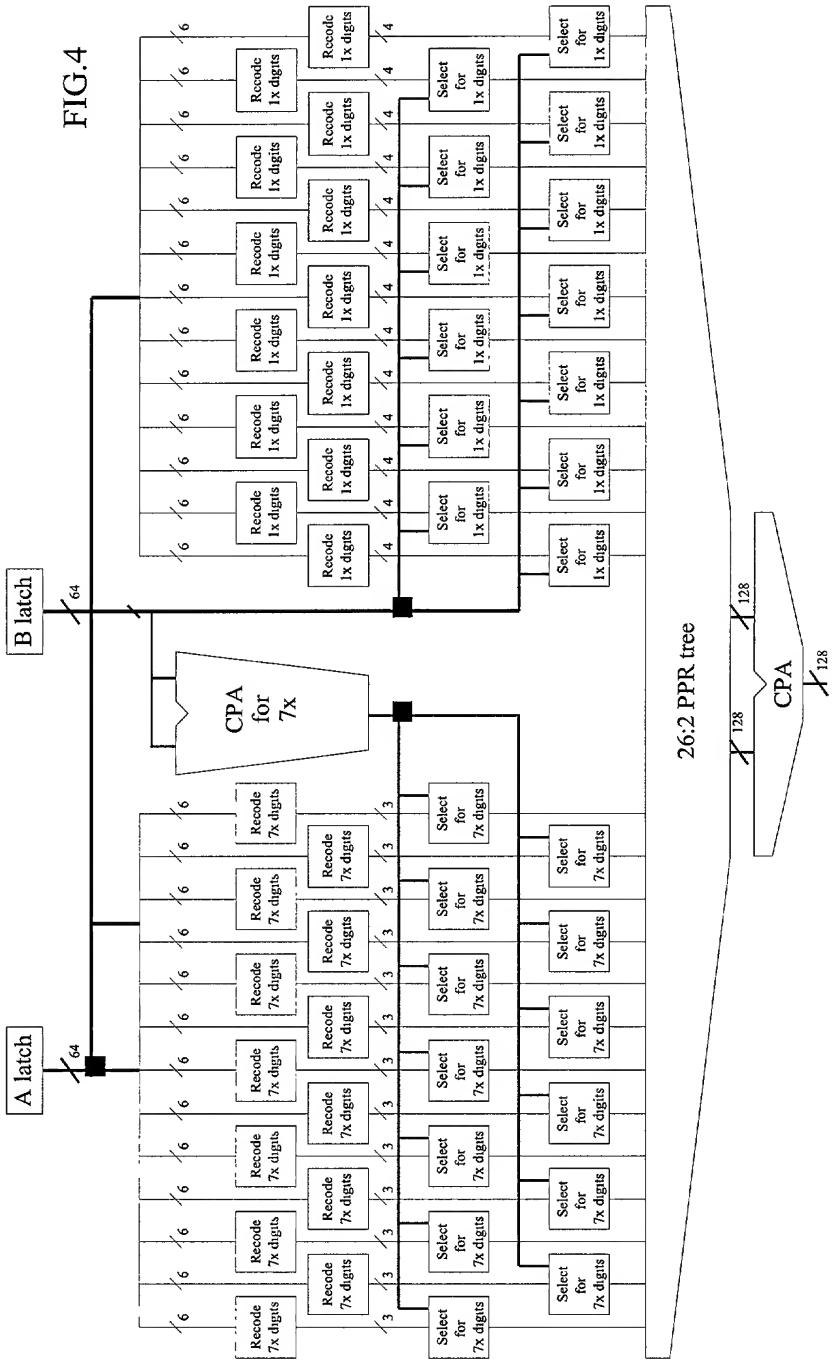

Figure 4: Block diagram of the precomputation option illustrating a further embodiment of the invention for a multiplier bit width of $p = 64$.